

Claims

- [c1] 1. A method of fabricating semiconductor wafers, comprising:
providing a plurality of semiconductor wafers, wherein the plurality of semiconductor wafers comprises a first semiconductor wafer and a second semiconductor wafer, and wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer;
providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials;
choosing a material from the plurality of materials existing in said relationship;
forming a substructure comprising the material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the of the second semiconductor wafer; and
placing the plurality of semiconductor wafers into a furnace for processing, wherein the furnace comprises an elevated temperature resulting in a value for the first semiconductor wafer of the electrical characteristic that corresponds to said material in said relationship.
- [c2] 2. The method of claim 1, wherein said forming the substructure comprises applying at least one layer of the material to the backside of the second semiconductor wafer.
- [c3] 3. The method of claim 1, wherein said forming the substructure comprises removing at least one layer of a first material from the backside of the second semiconductor wafer to expose the material.
- [c4] 4. The method of claim 1, wherein said forming the substructure comprises placing a monitor wafer comprising the material between the backside of the second semiconductor wafer and the topside of the first

semiconductor wafer.

- [c5] 5. The method of claim 1, wherein the material is selected from the group consisting of Si, Si₃N₄, and SiO₂.
- [c6] 6. The method of claim 5, wherein the furnace is a polysilicon LPCVD furnace.
- [c7] 7. The method of claim 6, wherein the electrical characteristic is polysilicon sheet resistance.
- [c8] 8. The method of claim 5, wherein the furnace is a gate oxidation furnace.
- [c9] 9. The method of claim 8, wherein the electrical characteristic is a gate oxide thickness.
- [c10] 10. The method of claim 1, wherein said relationship is a graphical relationship.
- [c11] 11. The method of claim 1, wherein said relationship is a tabular relationship.
- [c12] 12. A method of fabricating semiconductor wafers, comprising:
providing a plurality of semiconductor wafers, wherein the plurality of semiconductor wafers comprises a first semiconductor wafer, a second semiconductor wafer, a third semiconductor wafer, and a forth semiconductor wafer, wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer, and wherein the third semiconductor wafer is located adjacent to the forth semiconductor wafer;
providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials;
choosing a first material from the plurality of materials existing in said

relationship;
choosing a second material from the plurality of materials existing in said relationship;
forming a first substructure comprising the first material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the of the second semiconductor wafer;
forming a second substructure comprising the second material sandwiched between a topside of the third semiconductor wafer and a backside of a portion of the forth semiconductor wafer;
placing the plurality of semiconductor wafers into a furnace for processing, wherein the furnace comprises an elevated temperature resulting in a first value for the first semiconductor wafer of the electrical characteristic that corresponds to said first material in said relationship and a second value for the third semiconductor wafer of the electrical characteristic that corresponds to said second material in said relationship, and wherein the first value is not a same value as the second value.

- [c13] 13. The method of claim 12, wherein said forming the first substructure comprises applying at least one layer of the first material to the backside of the second semiconductor wafer, and wherein said forming the second substructure comprises applying at least one layer of the second material to the backside of the forth semiconductor wafer.
- [c14] 14. The method of claim 12, wherein said forming the first substructure comprises removing at least one layer of a third material from the backside of the second semiconductor wafer to expose the first material, and wherein said forming the second substructure comprises removing at least one layer of a forth material from the backside of the forth

semiconductor wafer to expose the second material.

- [c15] 15. The method of claim 12, wherein said forming the first substructure comprises placing a first monitor wafer comprising the first material between the backside of the second wafer and the topside of the first semiconductor wafer, and wherein said forming the second substructure comprises placing a second monitor wafer comprising the second material between the backside of the forth semiconductor wafer and the topside of the third semiconductor wafer.
- [c16] 16. The method of claim 12, wherein the first material and the second material are each selected from the group consisting of Si, Si₃N₄, and SiO₂.
- [c17] 17. The method of claim 16, wherein the furnace is a polysilicon LPCVD furnace.
- [c18] 18. The method of claim 17, wherein the electrical characteristic is polysilicon sheet resistance.
- [c19] 19. The method of claim 16, wherein the furnace is a gate oxidation furnace.
- [c20] 20. The method of claim 19, wherein the electrical characteristic is a gate oxide thickness.
- [c21] 21. The method of claim 12, wherein said relationship is a graphical relationship.
- [c22] 22. The method of claim 12, wherein said relationship is a tabular relationship.
- [c23] 23. An electrical structure, comprising:

a first semiconductor wafer;
a second semiconductor wafer; and
a first material, wherein the first material is sandwiched between a topside of the first semiconductor wafer and a backside of the second semiconductor wafer, wherein a relationship exists between a plurality of values for an electrical characteristic and a plurality of materials comprising the first material, and wherein the first semiconductor wafer comprises a discrete value from the plurality of values for the electrical characteristic that correlates with the first material in said relationship.

- [c24] 24. The electrical structure of claim 23, wherein the first material is attached to the backside of the second semiconductor wafer.
- [c25] 25. The electrical structure of claim 23, wherein the first material is selected from the group consisting of Si, Si₃N₄, and SiO₂.
- [c26] 26. The electrical structure of claim 23, wherein the electrical characteristic is polysilicon sheet resistance.
- [c27] 27. The electrical structure of claim 23, wherein the electrical characteristic is a gate oxide thickness.
- [c28] 28. The electrical structure of claim 23, wherein said relationship is a graphical relationship.
- [c29] 29. The electrical structure of claim 23, wherein said relationship is a tabular relationship.